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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,268	08/14/2006	Katsunori Asano	925-327	6483

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EXAMINER	
JAHAN, BILKIS	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
08/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,268	ASANO ET AL.	
	Examiner	Art Unit	
	BILKIS JAHAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-33* is/are pending in the application.

4a) Of the above claim(s) *20-23,26 and 30-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-19,24,25 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/14/06, 10/06/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election without traverse Species I, Fig. 2, claims 17, 18, 19, 24, 25, 27, 28 and 29 filed on 6/12/08 has been acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention because claim 24 depends on claim 23 which is another **species**. Therefore, claim 24 cannot be examined with the elected **species** independent claim 17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-19, 25, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oikawa et al (5,021,855) in view of Piccone et al (5,005,065).

Regarding claim 17, Oikawa et al disclose a gate turn-off thyristor of a wide-gap semiconductor (Fig. 1B), comprising:

- a first emitter layer 2 (Fig. 1B, col. 4, lines 38-39) of either one of n-type and p-type (Fig. 1B) conductive types having a first electrode 7 (Fig. 1B, col. 5, line 44) on its one surface (Fig. 1B);
- a first base layer 3 (Fig. 1B, col. 4, line 40) of a conductive type (Fig. 1B, n-type) different from that of the first emitter layer 2 (Fig. 1B, col. 4, lines 38-39) provided on the other surface of the first emitter layer 2 (Fig. 1B, col. 4, lines 38-39);
- a second base layer 4 (Fig. 1B, col. 4, line 42) of a conductive type identical to that of the first emitter layer 2 (Fig. 1B, col. 4, lines 38-39) provided on the first base layer 3 (Fig. 1B, col. 4, line 40);
- a mesa-type second emitter layer 5A-5B (Fig. 1B, col. 4, lines 57-59) of a conductive type different (Fig. 1B, n-type) from that of the first emitter layer 2 (Fig. 1B, col. 4, lines 38-39) provided in the second base layer 4 (Fig. 1B, col. 4, line 42);
- a second electrode 8A-8C (Fig. 1B, col. 5, lines 44-45) provided on the mesa-type second emitter layer 5A-5B (Fig. 1B, col. 4, lines 57-59); a low-resistance gate region 6 (Fig. 1B, col. 5, lines 3, 20-27) provided in the second base layer 4 (Fig. 1B, col. 4, line 42) below a bottom surface of a mesa (Fig. 1B) that surrounds the mesa-type second emitter layer 5A-5B (Fig.

1B, col. 4, lines 57-59) and having a conductive type identical to that of the second base layer 4 (Fig. 1B, col. 4, line 42) and an impurity concentration higher than that of the second base layer (col. 5, lines 33-36); and

- a third electrode 9 (Fig. 1B, col. 6, line 43) put in contact with the low-resistance gate region 6 (Fig. 1B, col. 5, lines 3, 20-27) via a gate contact region 6C (Fig. 4, col. 7, lines 57-58) but does not disclose the first emitter layer 2 provided on the second base layer 4.
- However, Piccone et al disclose the first emitter layer 18 (Fig. 11, col. 4, lines 37-38) provided on the second base layer 12 (Fig. 11). Piccone teaches the first emitter layer provided on the second base layer is used to reduce susceptibility to avalanching in a mode that can retrigger the miniature thyristor into conduction immediately following squeeze-off of current through the miniature thyristor by a gate signal (col. 2, lines 13-20). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Oikawa's structure with Piccone's structure including the first emitter layer provided on the second base layer to reduce susceptibility to avalanching in a mode that can retrigger the miniature thyristor into conduction immediately following squeeze-off of current through the miniature thyristor by a gate signal (col. 2, lines 13-20).

Regarding claim 18, Oikawa et al further disclose a low-resistance region is provided by making the low-resistance gate region 6 (Fig. 1B, col. 5, lines 3, 20-27) have an

impurity concentration in the neighborhood of the junction thereof with the third electrode 9 (Fig. 1B, col. 6, line 43) higher than an impurity concentration of the other portion of the low-resistance gate region (col. 5, lines 33-36).

Regarding claim 19, Oikawa et al further disclose the low-resistance gate region 6 (Fig. 1B, col. 5, lines 3, 20-27) is provided in the second base layer 4 (Fig. 1B, col. 4, line 42) in the neighborhood of the junction between the second emitter layer 5A-5B (Fig. 1B, col. 4, lines 57-59) and the second base layer 4 (Fig. 1B, col. 4, line 42).

Regarding claim 25, Oikawa et al further disclose the first emitter layer is an n-type cathode emitter layer 5A-5B (Fig. 1B, col. 4, lines 57-59), the first base layer 4 (Fig. 1B, col. 4, line 42) is a p- type base layer, the second base layer is an n-type base layer 3 (Fig. 1B, col. 4, line 40), the second emitter layer is a p-type anode emitter layer 2 (Fig. 1B, col. 4, lines 38-39), and the low-resistance gate region is an n-type 6 (Fig. 1B, col. 5, lines 3, 20-27), and the first, second and third electrodes are a cathode electrode 8A-8C (Fig.1B), an anode electrode 7 (Fig. 1B) and a gate electrode 9 (Fig. 1B), respectively (Fig. 1B).

Regarding claims 28, 29, Oikawa et al further disclose an impurity concentration of the low-resistance gate region is three or more times an impurity concentration of the base region (col. 5, lines 33-35).

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oikawa et al (5,021,855), Piccone et al (5,005,065) and further in view of Edmond et al (5,539,217).

Regarding claim 27, Oikawa et al further disclose limitations above but do not disclose the wide-gap semiconductor is silicon carbide (SIC). However, Edmond et al disclose the wide-gap semiconductor is silicon carbide (SIC) (Abstract). Edmond teaches SiC semiconductor is used to improve high thermal conductivity and high breakdown electric field in the device (col. 2, lines 25-28). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Oikawa in view of Piccone's structure with Edmond's structure including the wide-gap semiconductor is silicon carbide to improve high thermal conductivity and high breakdown electric field in the device (col. 2, lines 25-28).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ